

## Engineered Excellence

**SILVACO**

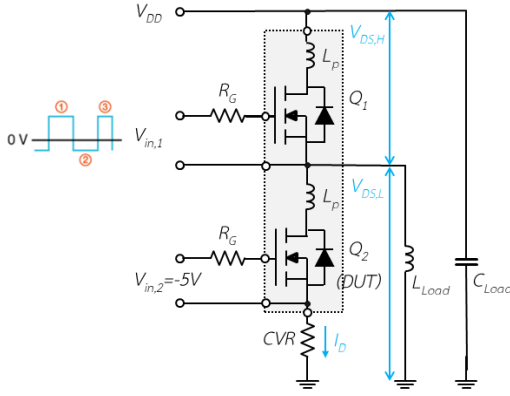


Figure 3: Dynamic testing circuit for a RR test with two power MOSFETs.

A negative voltage at the gate of Q2 switches the device off. Current conduction is only allowed through the intrinsic body-diode of that device. When doing actual measurements, this provides all transient data from the same device avoiding any effects from the differences between the two MOSFETs.

## Simulation Setup

The simulation flow for structure generation and meshing as well as the device simulations in mixed mode is implemented in Victory DoE, a user interface (UI) driven software solution to automate TCAD simulation projects, run experiments, and perform data analysis. The simulations are based on a SiC 1200V/25A power MOSFET device. The simulation flow starts with Victory Process, which simulates the process steps required to build a planar DMOS device. For a realistic doping profile, a Monte-Carlo ion implantation method is used. This is followed by a simulated anneal using an equilibrium activation model. The generated structure is imported into Victory Mesh, which rebuilds the mesh using a Delaunay meshing scheme, Figure 4. Special care has been taken to minimize the number of mesh nodes in the structure to facilitate efficient circuit simulation times.

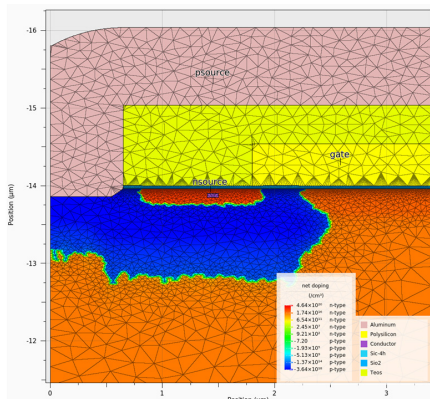


Figure 4: SiC MOSFET structure and Delaunay simulation mesh for device simulations containing ~6k nodes.

The switching characteristics of the device are simulated using Victory Device in transient mixed mode according to Figure 1 and 3. The circuit netlist is based on a bus voltage of  $V_{DD}=800V$ ,  $L_{Load}=250\mu H$ ,  $C_{Load}=40\mu F$ ; the gate resistance is limited to  $R_G=5...80\Omega$ . The two active MOSFET devices have an additional parasitic inductance connected to the drain contact ( $L_P=5nH$ ). Typical mixed-mode simulation times are observed to be of the order of a couple of hours, depending on the number of current oscillations in the output waveform.

## Simulation Method and Results

### (A) Double-Pulse Test (DPT)

Figure 5 shows the gate drive and resulting waveforms expected from the simulation of the DPT.

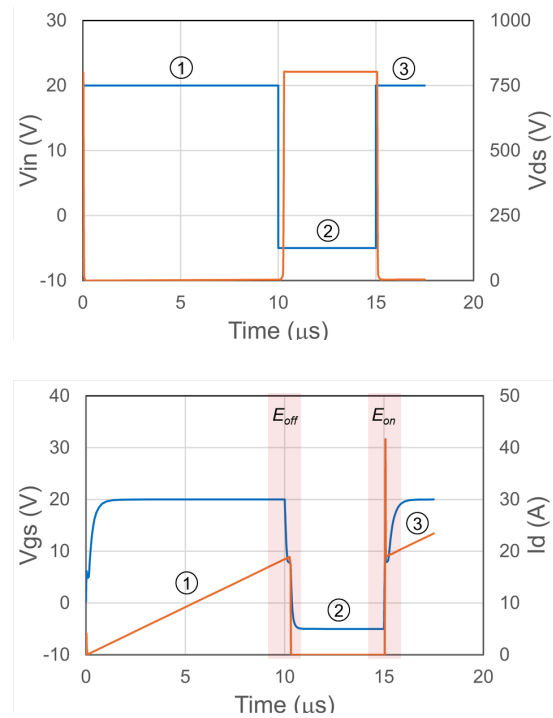


Figure 5: Schematics of gate drive (top) and expected waveforms (bottom) for the DPT test

Shown are three distinct regions of operation of the DUT. In region 1, the device is turned on and the current ( $I_D$ ) of the DUT begins to flow. The width of this pulse will set the targeted current for the device operation. Its duration can be calculated based on the voltage applied, the inductor value, and the targeted current value:

$$T(\text{pulse1}) = \frac{L_{Load}}{V_{DD}} * I(\text{target})$$

In region 2, the device is shut off for a short amount of time. In region 3, the device is turned on again and the current continues to increase. The pulse time in region 3 is much shorter than the one in region 1 to avoid

self-heating. Switching energies are extracted from the simulated waveforms, using the definitions from Figure 2. Key timing parameters and their definitions are listed in Table 1.

Timing parameter	
Delay on time	10% VGS -> 90% VDS
Rise time	90% VDD -> 10% VDS
On time	10% VGS -> 10% VDS
Delay off time	90% VGS -> 10% VDS
Fall time	10% VDS -> 90% VDS
Off time	90% VGS -> 90% VDS

Table 1: Definition of timing parameters for the DPT.

Additional performance characteristics are evaluated using the simulated DPT waveforms, specifically this includes switching losses, i.e. the energy required to turn the device on ( $E_{on}$ ) and off ( $E_{off}$ ). The calculation of these energy losses is based on the description provided in Figure 6.

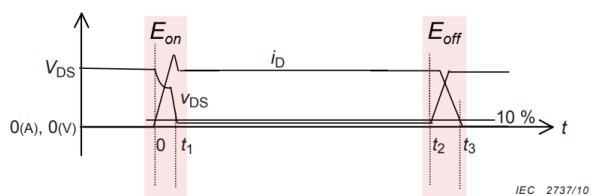


Figure 6: Switching energy extractions (from [1]).

The calculations are done by integrating over the output power from the DPT:

$$E_{on} = \int_0^{t1} I_D * V_{DS} * dt$$

$$E_{off} = \int_{t2}^{t3} I_D * V_{DS} * dt$$

Figure 6 shows the simulated  $I_D$  and  $V_{DS}$  waveforms used in the integration of  $E_{off}$  and  $E_{on}$ .

The DC figures of merit for the SiC MOSFET device are extracted from TCAD simulations for the single device. Extractions include  $R_{DS,on}$ ,  $V_{GS,th}$  and  $V_{br,DSS}$ . The mixed-mode simulation is then performed to extract the dynamic performance characteristics as described above. Note that  $E_{off}$  is calculated from the first turn-off and  $E_{on}$  is calculated from the second turn-on as seen in Figure 5 (bottom), assuring that the current in the device is the same for both calculations. Figure 7 shows the results of the DUT mixed-mode simulation for the circuit.

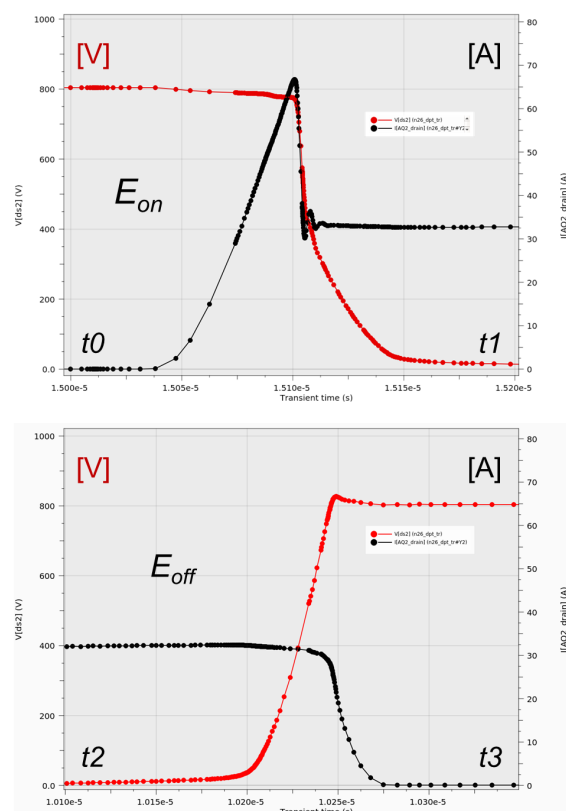


Figure 7: Simulated output waveforms  $I_D$  (black) and  $V_{DS}$  of Q2 (red) for  $E_{on}$  (top) and  $E_{off}$  (bottom) plotted with Victory Visual.

OUT:Vth.vpm	Vth_V	4.54
OUT:Rdson.vpm	Rdson_mOhm	73.4
OUT:Vbrdss.vpm	Vbrdss_V	2047.6
	Vgsmax_V	20.02
	Vdsmax_V	814.83
	t1_us	15.0268
	t2_us	15.1018
	t3_us	15.1361
	Ton_us	0.109303
	Tr_us	0.034259
	Tdon_us	0.075044
OUT:Switching.vpm	Eon_uJ	1705.81
	t4_us	10.0073
	t5_us	10.2076
	t6_us	10.2432
	Toff_us	0.235946
	Tf_us	0.035596
	Tdoff_us	0.20035
	Eoff_uJ	466.07
	Econd_uJ	2439.17

Figure 8: DC/AC and dynamic characteristics of the SiC MOSFET from a DPT simulation as appears in the Victory DoE results dialogue.

### (B) Reverse-Recovery (RR) Test

The reverse-recovery simulations according to Figure 2, are performed in a similar way. The load inductor is now across the DUT (Q2). First the DUT is shut off by applying a negative voltage to the MOSFET gate. The Q1 is actively switched by applying the input waveform, Figure 9 (top). This allows the body-diode to be characterized. The switching sequence for the RR test is identical to that of the DPT. The analysis focusses on the switching-off losses as the dominant component, Figure 9 (top). The body-diode of Q2 starts the reverse recovery when Q1 is turned on. As in the DPT, the recovery current ( $I_d$ ) is detected as the current through a current-visualization resistor (CVR) which is placed in series with the DUT.

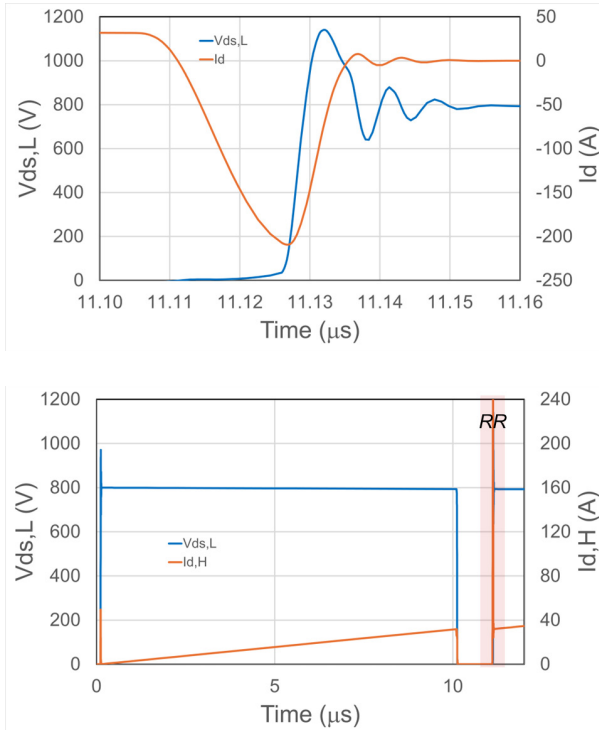


Figure 9: Schematics of gate drive (top) and expected waveforms (bottom) for the RR test.

Parameters extracted are the peak drain voltage ( $V_{rm}$ ) and the maximum current ( $I_{rm}$ ) at diode recovery. In particular, the  $V_{rm}$  spike can exceed  $V_{DD}$  by a large amount leading to catastrophic loss of the device. Also, extracted is the recovery time  $T_{rr}$ , defined as the time difference between the initial point where the  $I_d$  waveform goes through zero ( $t1$ ) and the next point of zero current ( $t3$ ), as shown in Figure 10. The integral under that curve segment is called the reverse-recovery charge,  $Q_{rr}$ . This is the electric charge which is removed during the reverse-recovery process, i.e.

$$Q_{rr} = \int_{t1}^{t3} I_D * dt$$

The softness factor, or snappiness of the recovery is calculated as:

$$S = \frac{T_b}{T_a}$$

Where  $T_a$  is the portion of the time  $T_{rr}$  needed to reach  $I_{rm}$  (at  $t2$ ) from  $t1$  and  $T_b$  is the time to  $t3$ . For  $S=1$ , the current flow into and out of the body diode is equivalent. A snappy recovery is observed if  $S \gg 1$ . For  $S < 1$ , one speaks of soft recovery.

Snappiness can be defined in various ways; another method uses the ratio of the current derivatives at  $t1$  ( $sf$ ) and close to  $t3$  ( $sr$ ). Figure 11 shows the results of the RR simulations.

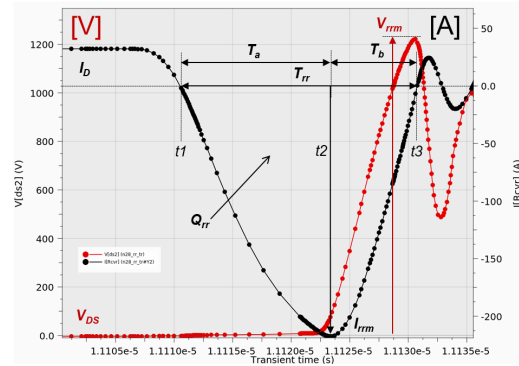


Figure 10: Simulated output waveforms  $I_d$  (black) and  $V_{DS}$  of Q2 (red) plotted with Victory Visual.

OUT:Qrr.vpm	Vrrm_V	1220.7
	Irrm_A	217.7
	t1_us	11.1105
	t2_us	11.1234
	t3_us	11.1308
	Trr_ns	20.27
	Ta_ns	12.84
	Tb_ns	7.44
	Qrr_nC	2693.2
	S	0.579
	sf	1.75E+10
	sr	4.28E+10

Figure 11: Simulated dynamic characteristics of the SiC MOSFET from a RR simulation as appears in the Victory DoE results dialogue.

## Conclusion

Semiconductor power transistors operate exclusively in switching circuits. Packaged into modules, the task for the design engineer is to characterize modules rather than amplifying the importance of a single design parameter such as  $R_{ds(on)}$ . The Silvaco TCAD software, and in particular the device simulator Victory Device in mixed mode are uniquely placed to address these design tasks. In this paper, MOSFET switching (DPT) and diode reverse-recovery (RR) simulations have been carried out. We discussed the simulation setup and extraction methodology in detail.

## Reference

- [1] Semiconductor devices – Discrete Devices, Part 8: Field effect transistors, International standard IEC 60747-8:2010/AMD1:2021.